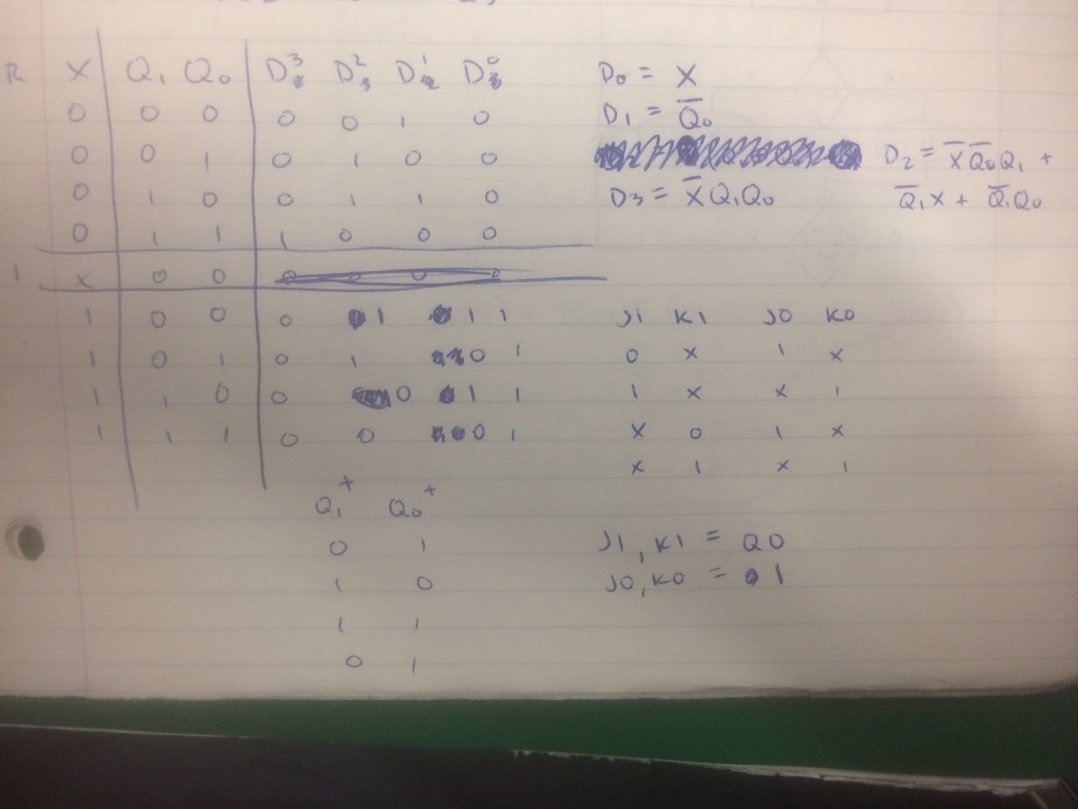
Lab 7 Summary

Irvin, Mitchell

Section 7441

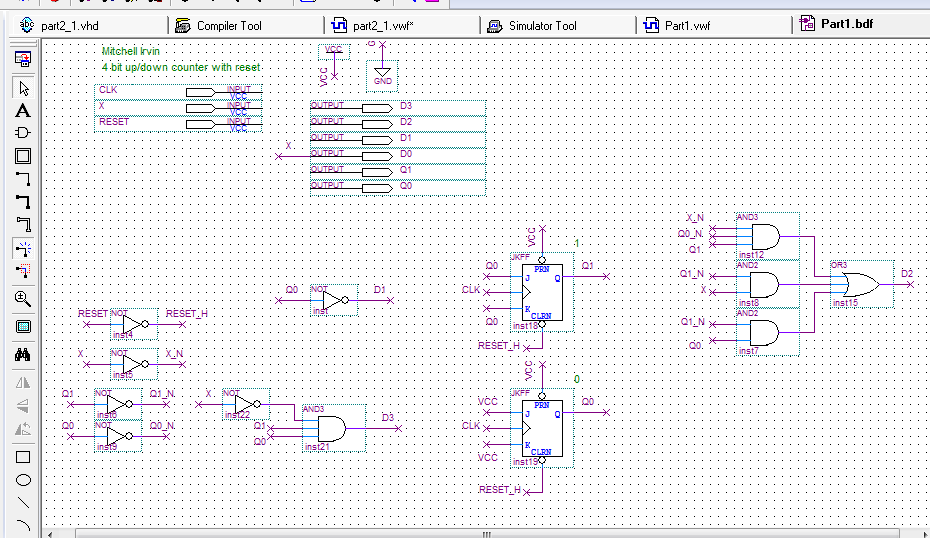
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PART 1

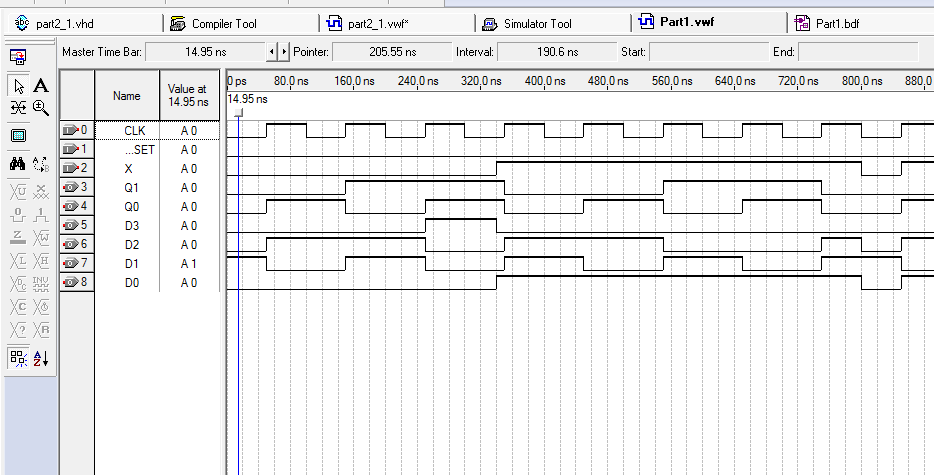


Next state table for part 1 (counter) w/ simplified equations

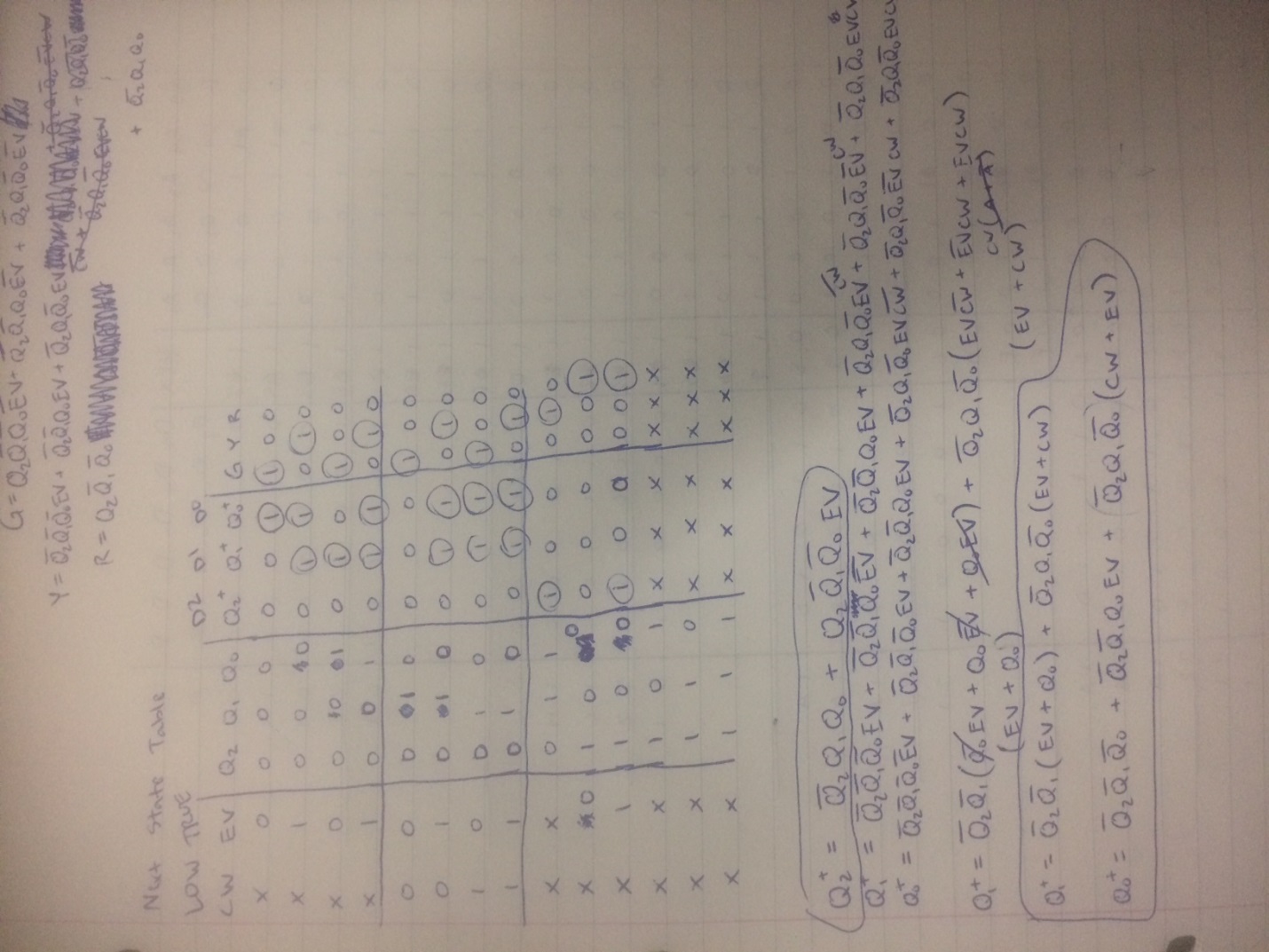
BDF for counter



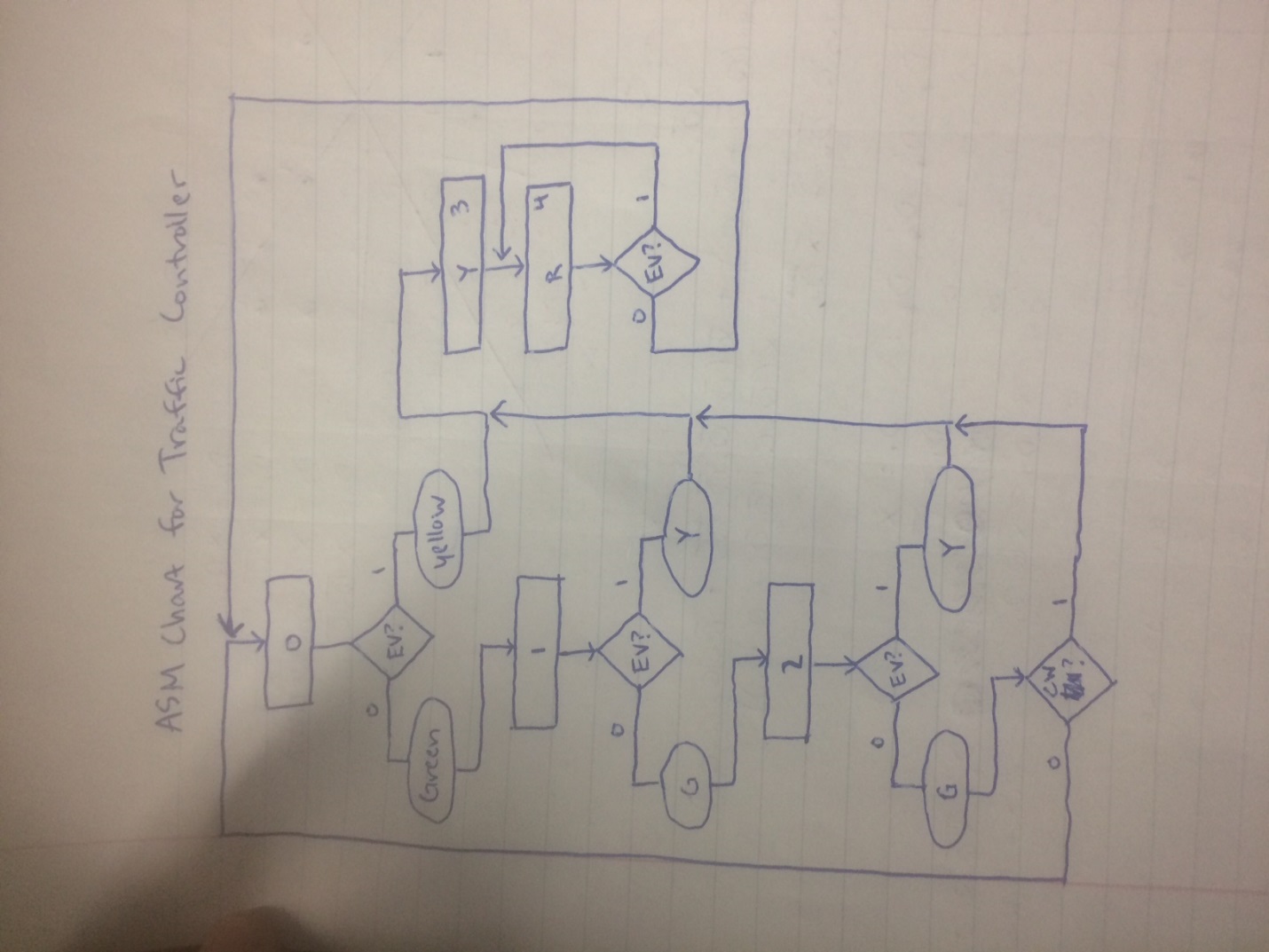
VWF simulation for counter



PART 2

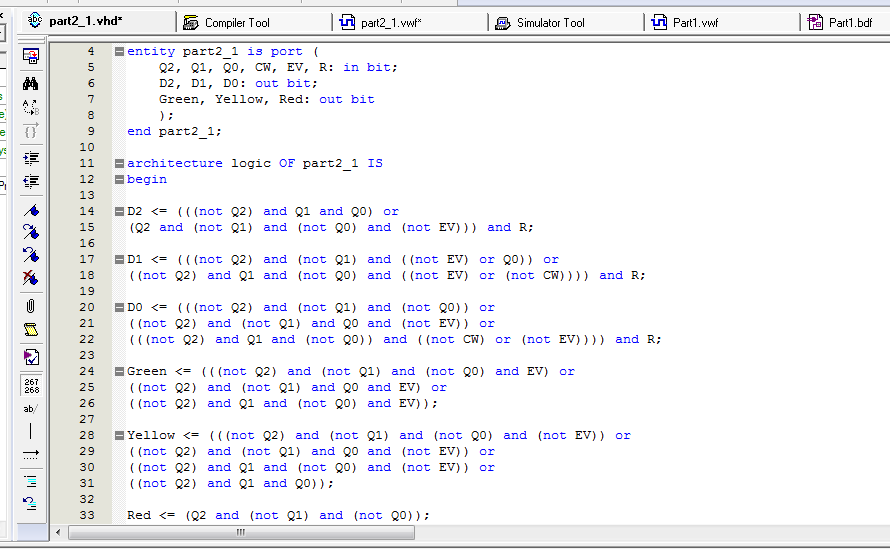


next state table and simplified equations

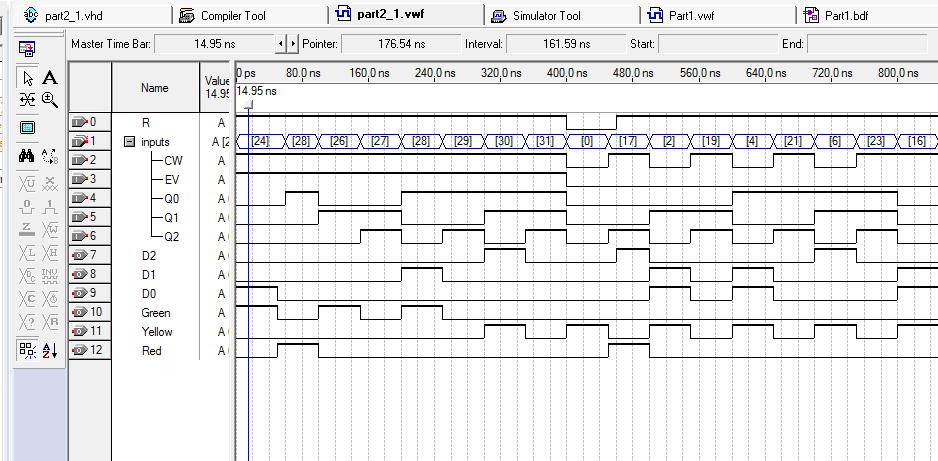


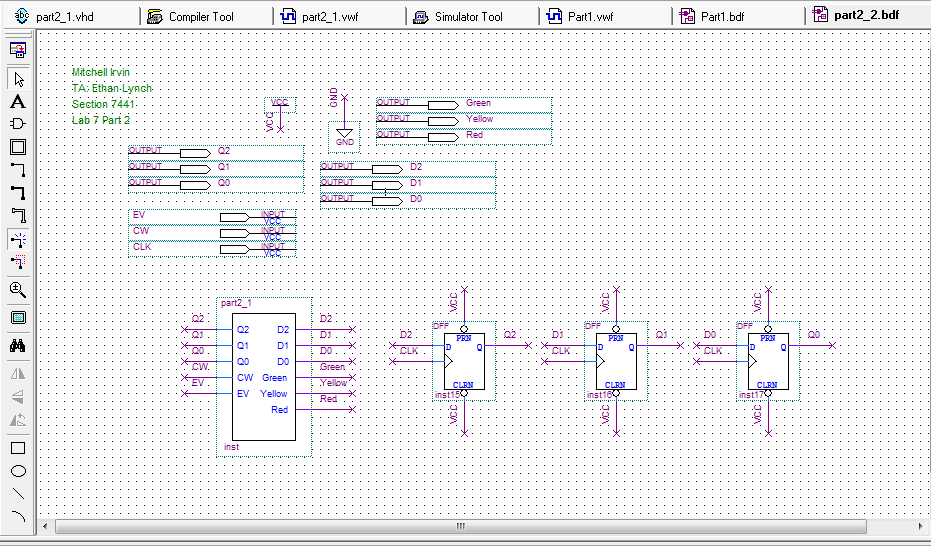
the ASM for the logic of part 2

VHD for part 2 logic

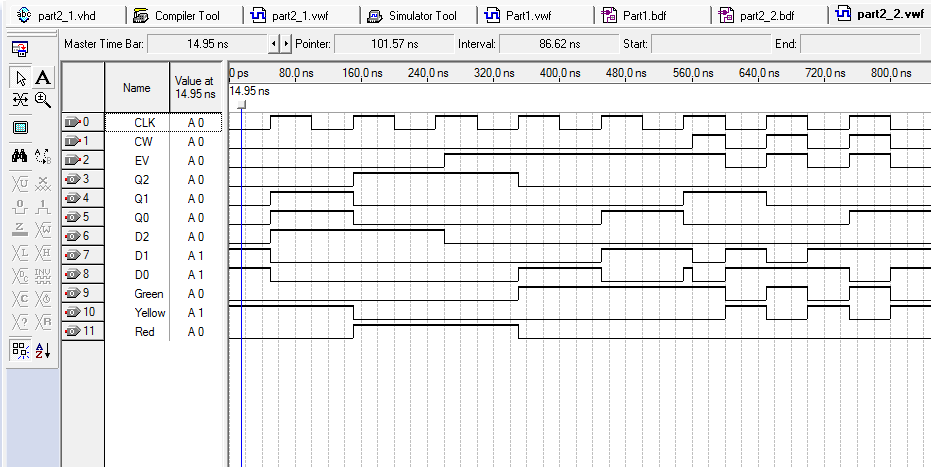


VWF for part 2 logic





Part 2 implementation bdf



Part 2 implementation VWF

Memory table w/ addresses and Data bits

